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1 14. (Amended) The memory module controller of claim 13, further comprising;
2 second interface circuitry coupled to the control logic and configured to
3 receive from one of the plurality of memory devices a second memory transaction
4 in a second format, wherein the control logic reformats the second memory
5 transaction [for the system memory bus] such that the system memory controller
6 performs the reformatted second memory transaction.

REMARKS

Reconsideration of this application, as amended, is respectfully requested. The following remarks are responsive to the Office Action mailed on September 13, 1999.

The specification is objected for minor informalities. The title of the invention is objected to as being non-descriptive. The abstract is objected to because of minor informalities.

Claims 1, 12, and 13 stand objected to for minor informalities.

Claims 1-14 stand rejected under 35 U.S.C. §102(b) as being unpatentable over Memory Systems Design and Applications, edited by Dave Bursky, pp. 213-220 ("Bursky").

Claims 1-14 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-17 of copending Application No. 09/023,234 and claims 1-20 of copending Application No. 09/023,170.

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Claims 1-14 are pending. Claims 1-14 have been amended. Applicant respectfully submits that the amendments made herein do not add new matter.

The Examiner has objected to the specification on page 2 for having missing serial numbers. Accordingly, the specification has been amended to provide the appropriate missing serial numbers.

The Examiner has objected to the title of the invention as being non-descriptive. Accordingly, the title of the invention has been amended. Applicant respectfully submits that the amended title is clearly indicative of the invention which the claims are directed.

The Examiner has objected to the abstract. In particular, the Examiner has objected to the term "system memory module," and requests appropriate correction or clarification. Accordingly, the Abstract has been replaced with a new Abstract attached herewith.

The Examiner has objected to claims 1, 12, and 13 for minor informalities. In particular, the Examiner states:

It is not clear to the Examiner what is meant by the phrase "system memory module" in lines 2 and 3 of each claim.

(p.2 Office Action 09/13/99).

Applicant respectfully submits that claims 2 and 3, as amended, overcome the Examiner's objection.

The Examiner has rejected claims 1-14 under 35 U.S.C. §102(b) as being unpatentable over Bursky. In particular, the Examiner states:

Regarding claims 1, 2, and 12-14, on page 217 Bursky teaches in the photo caption that "System costs plummet when

function duplication is designed out. While most minis duplicate read/write and control electronics for each board of memory DIPs, Interdata makes one read/write/control set serve more memory, by using eight little 'daughter boards.' The packaging also simplifies reconfiguration and speeds up field repair" (emphasis added).

Furthermore, on page 219, third column, he writes that "The PC-board economy is possible through the use of 'daughter boards,' strips that are 8 in. long, 1 in. wide and plug into the 15x15 in. memory board itself. Not only does this mean that 256 k-bytes can be packed on the board instead of 32 or 64 k-bytes, it also means that function duplication is cut back. As a result, the read/write control logic that would have been duplicated on a series of 64 k-byte boards appears just once on the 15x15 in. motherboard, serving all 256 k-bytes. Larry MacPherson, Interdata product manager for the Series Sixteen, points out that this unusual modularity makes it easy to add and subtract memory in the field, and slashes the cost of incremental memory increases" (emphasis added).

Bursky's focus in the passages above is toward the daughter card system of Interdata. However, the underlined passage above teach that it was known to use memory controllers on individual memory modules, each of which contained a plurality of memory device as claimed. In fact, such a design appears to have been the norm. The passages above describe a new (for the time) method of reducing the duplication of the memory controllers by removing them from the memory modules and using a single controller on the motherboard for all memory modules (daughter cards). This is the standard today, and is the admitted prior art of the instant application. However, in 1980 and before, it was common to include the memory controller an each memory module as taught above.

Bursky does not explicitly teach that the memory controller reformats the transactions it receives before passing them on to the plurality of memory devices, however such reformatting is inherent in the devices described by Bursky since memory devices required different format signals than memory module controllers. Bursky does not characterize the memory controllers of the memory modules other than to call them read/write/control logic, which meets the broad claim language of handling requests (reads or writes) and controlling transactions.

(pp.4-5 Office Action 9/13/99).

Applicant respectfully submits that claim 1, as amended, is not anticipated by Bursky. Claim 1 includes the limitation of:

A memory module controller for providing an interface between a system memory controller and a plurality of memory devices on a memory module, comprising:
first interface circuitry configured to receive from the system memory controller a first memory transaction in a first format; and
control logic coupled to the first interface circuitry and configured to convert the first memory transaction into a second memory transaction in a second format for the plurality of memory devices, wherein the second format of the second memory transaction is different from the first format of the first memory transaction.

(Claim 1)(emphasis added).

In contrast to claim 1, Bursky fails to disclose or suggest a memory module controller having control logic coupled to the first interface circuitry and configured to convert the first memory transaction into the second memory transaction in a second format for the plurality of memory devices, and the second format of the second memory transaction is different from the first format of the first memory transaction.

Bursky relates generally to providing reliability to memory devices by using error correction capability. See Bursky pp.216-200. The Examiner, however, relies on the following sections of Bursky to support the §102(b) rejection.

System costs plummet when function duplication is designed out. While most minis duplicate read/write and control electronics for each board of memory DIPS, Interdata makes one read/write/control set serve more memory, by using eight little "daughter boards." This packaging also simplifies reconfiguration and speeds up field repair.

(Bursky p.217, photo caption text).

The PC-board economy is possible through the use of "daughter boards," strips that are 9-in. long, 1-in. wide and plug into the 15x15-in. memory board itself. Not only does this mean that 256 kbytes can be packed on the board instead of 32 or 64 kbytes, it also means that function duplication is cut back.

As a result, the read/write control logic that would have been duplicated on a series of 64-kbyte boards appears just once on the 15x15-in. motherboard, serving all 256 kbytes.

(Bursky p.219).

Applicant respectfully submits that the above sections of Bursky do not teach or suggest converting a first memory transaction in a first format into a second memory transaction in a second format by a memory module controller for a plurality of memory devices. The Examiner asserts that the read/write/control logic of Bursky inherently teach reformatting of transactions. It is respectfully submitted that this assertion is unsupported. The read/write/control logic taught by Bursky is used to perform read and write transactions for memory devices. Furthermore, Bursky provides no teaching whatsoever of converting a memory transaction in one format into another format.

For the above reasons, applicant respectfully submits that claim 1 is not anticipated by Bursky, and is in condition of allowance. Given that claims 2-11 depend directly or indirectly on claim 1, applicant respectfully submits that claims 2-11 are not anticipated by Bursky, and are in condition of allowance for the same reasons as claim 1.

Applicant respectfully submits that claim 12, as amended, is not anticipated by Bursky. Claim 12 includes the limitations of:

A memory module controller for providing an interface between a system memory controller and a plurality of memory devices on a memory module, comprising:

means for receiving from the system memory controller a first memory transaction in a first format; and

means for converting the first transaction into a second memory transaction in a second format for the plurality of memory devices, wherein the second format of the second memory transaction is different from the first format of the first memory transaction.

(Claim 12)(emphasis added).

In contrast to claim 12, Bursky fails to disclose or suggest a memory module controller having means for converting the first transaction into a second memory transaction in a second format for the plurality of memory devices, and the second format of the second memory transaction is different from the first format of the first memory transaction. As stated previously, Bursky provides no teaching or suggestion of converting memory transactions in one format to another format.

For the above reasons, claim 12 is not anticipated by Bursky, and is in condition of allowance.

Applicant respectfully submits that claim 13, as amended, is not anticipated by Bursky. Claim 13 includes the limitations of:

A memory module controller for providing an interface between a system memory controller and a plurality of memory devices on a memory module comprising:

first interface circuitry configured to receive from the system memory controller a first memory transaction in a first format; and control logic coupled to the first interface circuitry and configured to reformat the first memory transaction such that the

plurality of memory devices perform the reformatted first memory transaction.

(Claim 13)(emphasis added).

In contrast to claim 13, Bursky fails to disclose or suggest a memory module controller having control logic coupled to the first interface circuitry and configured to reformat the first memory transaction such that the plurality of memory devices perform the reformatted first memory transaction. Bursky is also not related to reformatting memory transactions.

For the above reasons, claim 13 is not anticipated by Bursky, and is in condition of allowance. Given that claim 14 depends on claim 13, applicant respectfully submits that claim 14 is not anticipated by Bursky, and is in condition of allowance for the same reasons as claim 13.

The Examiner has provisionally rejected claims 1-14 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-17 of copending Application No. 09/023,234 and claims 1-20 of copending Application No. 09/023,170.

Upon a condition of allowance of one or more claims, applicant will submit a terminal disclaimer for this application.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the rejections and objections set forth in the Office Action mailed September 13, 1999 have been overcome. Accordingly, applicant respectfully request that claims 1-14, as amended, be found in a condition of allowance.

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If a telephone interview will expedite the prosecution of the application,
the Examiner is invited to contact Mike Kim at (408) 720-8300 x345.

If there are any additional charges, please charge them to Deposit
Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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